### Implementing Cache Coherence

- Coherence protocols must enforce two rules:
  - **Write propagation**: Writes eventually become visible to all processors
  - **Write serialization**: Writes to the same location are serialized (all processors see them in the same order)

- How to ensure write propagation?
  - **Write-invalidate protocols**: Invalidate all other cached copies before performing the write
  - **Write-update protocols**: Update all other cached copies after performing the write

- How to ensure write serialization?
  - **Snooping-based protocols**: All caches observe each other’s actions through a shared bus
  - **Directory-based protocols**: A coherence directory tracks contents of private caches and serializes requests

### Snooping-Based Coherence

- Bus provides serialization point
  - Broadcast, totally **ordered**
  - Each cache controller “snoops” all bus transactions
  - Controller updates state of cache in response to processor and snoop events and generates bus transactions

- Snoopy protocol (FSM)
  - State-transition diagram
  - Actions

**MSI State Transition Diagram**

**MESI State Transition Diagram**
**Problem 1.**

Consider a multicore processor with multiple threads each running on a different core. The threads access a shared memory that holds their code and data. Note that each thread has been given a different region of the shared memory to hold its stack.

In lecture we introduced a new instruction SWAP that supports an atomic read-modify-write operation on a memory location, where the processor’s cache coherence protocol guarantees that no other SWAP operation can access the same memory location at the same time.

\[
\text{SWAP(Ra, literal, Rc)} \\
\text{PC} \leftarrow \text{PC} + 4 \\
\text{EA} \leftarrow \text{Reg}[Ra] + \text{literal} \\
\text{TMP} \leftarrow \text{Mem}[EA] \quad // \text{atomic with following line} \\
\text{Mem}[EA] \leftarrow \text{Reg}[Rc] \quad // \text{atomic with preceding line} \\
\text{Reg}[Rc] \leftarrow \text{TMP}
\]

The SWAP instruction can implement mutual exclusion as using the memory location `lock` as a binary semaphore.

\[
\text{CMOVE(0,R0)} \quad // \text{WAIT operation on lock} \\
\text{loop: SWAP(R31, lock, R0)} \\
\text{BEQ(R0, loop)} \\
\]

... critical section ...

\[
\text{CMOVE(1,R0)} \quad // \text{SIGNAL operation on lock} \\
\text{ST(R0, lock, R31)}
\]

Using the SWAP instruction to implement mutual exclusion as shown above, write code sequences for the more general `Signal(s)` and `Wait(s)` operations on an integer semaphore `s`, where `s:` is location in the shared memory. The goal is to ensure correct operation of `Signal(s)` and `Wait(s)` even if different cores are running the `Signal` or `Wait` code at the same time.

<table>
<thead>
<tr>
<th>Code for Wait(s):</th>
<th>Code for Signal(s):</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>
Problem 2.

Snoopy coherence protocols rely on broadcast communication to detect sharing and updates. These are conventionally implemented using bus networks that allow for one message to be sent at a time to all nodes on the network.

(A) Ben Bitdiddle is implementing a bus-based snoopy coherence protocol. One fifth of instructions access memory, and one quarter of these miss in the core’s local cache (either because the line is invalid or doesn’t have necessary permissions). Assuming each memory operation consists of a request and acknowledgement, the network traffic per core is therefore:

\[
\frac{1}{5} \cdot \frac{1}{4} \cdot 2 = \frac{1}{10} \text{ messages/instruction}
\]

Assume all bus messages take a single cycle. Considering only the message carrying capacity of the shared bus, how many cores can the bus support?

(B) Ben needs to build a larger system than the bus network will allow, so he changes the system to use a unidirectional ring network. In this design, the core issuing the memory operation sends the request around the ring, and each node along the way either forwards the request or replaces it with its response. Assuming a single-cycle per hop in the network, at how many cores will this design saturate?
Problem 3.

Ben Bitdiddle is designing a snoopy-based, write-invalidate MSI protocol for write-back caches. Suppose processors P1 and P2 are have private, snoopy caches. Both caches are initially empty. Consider the following sequence of accesses:

I₀ P2: read A
I₁ P1: write A
I₂ P2: read A
I₃ P1: write A
I₄ P2: read A
I₅ P2: read B
I₆ P2: read A

(A) Assume blocks A and B do not conflict in the cache. Using the MSI protocol, fill in the following table showing the cache line states for A and B after each access.

<table>
<thead>
<tr>
<th>Access</th>
<th>Shared bus transaction</th>
<th>Processor P1’s cache</th>
<th>Processor P2’s cache</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial state</td>
<td></td>
<td>A: I  B: I</td>
<td>A: I  B: I</td>
</tr>
<tr>
<td>After P2 reads A</td>
<td></td>
<td>A: I  B: I</td>
<td>A: S  B: I</td>
</tr>
<tr>
<td>After P1 writes A</td>
<td></td>
<td>A: B  B: I</td>
<td>A: B</td>
</tr>
<tr>
<td>After P2 reads A</td>
<td></td>
<td>A: B  B: I</td>
<td>A: B</td>
</tr>
<tr>
<td>After P1 writes A</td>
<td></td>
<td>A: B  B: I</td>
<td>A: B</td>
</tr>
<tr>
<td>After P2 reads A</td>
<td></td>
<td>A: B  B: I</td>
<td>A: B</td>
</tr>
<tr>
<td>After P2 reads B</td>
<td></td>
<td>A: B  B: I</td>
<td>A: B</td>
</tr>
<tr>
<td>After P2 reads A</td>
<td></td>
<td>A: B  B: I</td>
<td>A: B</td>
</tr>
</tbody>
</table>

(B) If Ben switches to a MESI protocol, which bus transactions and cache states would be different?

(C) Briefly describe a scenario where the additional E state in the MESI protocol would eliminate a shared bus trans
Problem 4.

We want to study the tradeoffs between the standard directory-based MSI and MESI coherence protocols. The state transition diagrams for the two protocols are shown on the front page of this handout.

(A) Consider the four-core system below. Each core has a private cache, and caches are kept coherent with a directory protocol. Each core runs a thread that issues a load followed by a store to a single address, as shown below. Each thread accesses a different address (core 1’s thread accesses A, core 2’s thread accesses B, etc.). These thread-private addresses are on different cache lines. The number in parenthesis indicates the global order of the accesses (i.e. LD A happens before ST A, which happens before LD B, etc.). Each access completes before the next one begins.

<table>
<thead>
<tr>
<th>Cache 1</th>
<th>Cache 2</th>
<th>Cache 3</th>
<th>Cache 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core 1</td>
<td>Core 2</td>
<td>Core 3</td>
<td>Core 4</td>
</tr>
</tbody>
</table>

(1) LD A
(2) ST A
(3) LD B
(4) ST B
(5) LD C
(6) ST C
(7) LD D
(8) ST D

For this sequence of 8 accesses, provide in the table below the total number of each type of bus requests for the MSI and MESI protocols. Assume all caches are initially empty, i.e., the initial states for each cache line is “I”.

<table>
<thead>
<tr>
<th>Protocol</th>
<th># of BusRd</th>
<th># of BusRdX</th>
<th># of BusWB</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSI</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MESI</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(B) Consider a different program where each thread reads globally shared data, as shown below.

<table>
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<th>Cache 3</th>
<th>Cache 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core 1</td>
<td>Core 2</td>
<td>Core 3</td>
<td>Core 4</td>
</tr>
</tbody>
</table>

(1) LD A
(2) LD A
(3) LD A
(4) LD A

For this sequence of 4 accesses, fill in the table below for the MSI and MESI protocols. Ignore coherence responses. Assume all caches are initially empty.

<table>
<thead>
<tr>
<th>Protocol</th>
<th># of BusRd</th>
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