CMOS Technology

• Qualitative MOSFET model
• CMOS logic gates
• CMOS design issues

Today’s handouts:
• Lecture slides

Notes:
• Lab #1 due Thu next week
Combinational Device Wish List

- Design our system to tolerate some amount of error
  ⇒ Add positive noise margins
  ⇒ VTC: gain > 1 & nonlinearity
- Lots of gain ⇒ big noise margin
- Cheap, small
- Changing voltages will require us to dissipate power, but if no voltages are changing, we’d like zero power dissipation
- Want to build devices with useful functionality (what sort of operations do we want to perform?)
A Deep Dive Into a Chip

Packaged chip

Silicon die (100-400mm²)

Transistor (MOSFET)

Die cross-section

6-15 metal layers (wires)

Source: Intel
N-Channel MOSFET: Physical View

MOSFETs (metal-oxide-semiconductor field-effect transistors) are four-terminal voltage-controlled switches. Current flows between the diffusion terminals (source and drain) if the voltage on the gate terminal is large enough to create a conducting “channel”, otherwise the MOSFET is off and the diffusion terminals are not connected.

Very thin (<20Å) high-quality SiO₂ insulating layer isolates gate from channel region.

Doped p-type silicon substrate

Heavily doped n-type diffusions

Channel region: electric field from charges on gate locally “inverts” type of substrate to create a conducting channel between source and drain.

I_{DS} \propto W/L

source

gate

drain

bulk

Metal gate

Inter-layer SiO₂ insulation

I_{DS} \propto W/L

Doped p-type silicon substrate
N-Channel MOSFET: Electrical View

The four terminals of a Field Effect Transistor (gate, source, drain and bulk) connect to conductors that generate a set of electric fields in the channel region which depend on the relative voltages of each terminal.

Want $V_P \leq V_N$
N-channel MOSFET $I_{DS}$ vs. $V_{DS}$

Ohmic: $I_{DS} = \frac{V_{DS}}{R}$

- $V_{GS} = 1000\text{mV}$
- $V_{TH} = 0.5V$
- Increasing $V_{GS}$
  - $900\text{mV}$
  - $800\text{mV}$
  - $700\text{mV}$
  - $600\text{mV}$
FETs Come in Two Flavors

NFET: n-type source/drain diffusions in a p-type substrate. Positive threshold voltage; inversion forms n-type channel.

PFET: p-type source/drain diffusions in a n-type substrate. Negative threshold voltage; inversion forms p-type channel.

The use of both NFETs and PFETs – complementary transistor types – is a key to CMOS (complementary MOS) logic families.
CMOS Recipe

If we follow two rules when constructing CMOS circuits, we can model the behavior of the mosfets as simple *voltage-controlled switches*:

**Rule #1**: only use NFETs in pulldown circuits
**Rule #2**: only use PFETs in pullup circuits

**NFET Operating regions:**

- "off": $V_{GS} < V_{TH,NFET}$
- "on": $V_{GS} > V_{TH,NFET}$

NFET threshold = $\sim 0.5 \text{V}$

**PFET Operating regions:**

- "off": $V_{GS} > V_{TH,PFET}$
- "on": $V_{GS} < V_{TH,PFET}$

PFET threshold $\sim -0.5 \text{V}$
When $V_{IN}$ is low, the nfet is off and the pfet is on, so current flows into the output node and $V_{OUT}$ eventually reaches $V_{DD}$ ($> V_{OH}$) at which point no more current will flow.

When $V_{IN}$ is high, the pfet is off and the nfet is on, so current flows out of the output node and $V_{OUT}$ eventually reaches GND ($< V_{OL}$) at which point no more current will flow.

When $V_{IN}$ is in the middle, both the pfet and nfet are “on” and the shape of the VTC depends on the details of the devices’ characteristics. CMOS gates have very high gain in this region (small changes in $V_{IN}$ produce large changes in $V_{OUT}$) and the VTC is almost a step function.
Beyond Inverters:
Complementary pullups and pulldowns

Now you know what the “C” in CMOS stands for!

We want *complementary* pullup and pulldown logic, i.e., the pulldown should be “on” when the pullup is “off” and vice versa.

<table>
<thead>
<tr>
<th>pullup</th>
<th>pulldown</th>
<th>F(inputs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>on</td>
<td>off</td>
<td>driven “1”</td>
</tr>
<tr>
<td>off</td>
<td>on</td>
<td>driven “0”</td>
</tr>
<tr>
<td>on</td>
<td>on</td>
<td>driven “X”</td>
</tr>
<tr>
<td>off</td>
<td>off</td>
<td>no connection</td>
</tr>
</tbody>
</table>

Since there’s plenty of capacitance on the output node, when the output becomes disconnected it “remembers” its previous voltage -- at least for a while. The “memory” is the load capacitor’s charge. Leakage currents will cause eventual decay of the charge (that’s why DRAMs need to be refreshed!).
CMOS Complements

- Conducts when $A$ is high: $A$
- Conducts when $A$ is low: $\overline{A}$

- Conducts when $A$ is high and $B$ is high: $A \cdot B$
- Conducts when $A$ is low or $B$ is low: $\overline{A} + \overline{B} = \overline{A \cdot B}$

- Conducts when $A$ is high and $B$ is high: $A + B$
- Conducts when $A$ is low or $B$ is low: $\overline{A} \cdot \overline{B} = \overline{A + B}$
A Pop Quiz!

What function does this gate compute?

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Current technology: $\lambda = 14$nm

COST for an older 45nm process:
- $3500$ per 300mm wafer
- 300mm round wafer = $\pi(150e^{-3})^2 = 0.07m^2$
- NAND gate = $(82)(16)(45e^{-9})^2 = 2.66e^{-12}m^2$
- $2.6e^{10}$ NAND gates/wafer (= 100 billion FETS!)
- marginal cost of NAND gate: $132n$
General CMOS Gate Recipe

Step 1. Figure out the pullup network that does what you want, e.g.,

\[ F = \overline{A} + \overline{B} \times \overline{C} \]

(Determine what combination of inputs generates a high output)

Step 2. Walk the hierarchy replacing PFETs with NFETs, series subnets with parallel subnets, and parallel subnets with series subnets

Step 3. Combine PFET pullup network from Step 1 with NFET pulldown network from Step 2 to form a fully-complementary CMOS gate.

Does this recipe work for all logic functions?
CMOS Gates Are Naturally Inverting

In a CMOS gate, rising inputs (0→1) lead to falling outputs

- NFETs go from “off” to “on”
  → pulldown paths connected
  → output may be connected to ground

- PFETs go from “on” to “off”
  → pullup paths disconnected
  → output may be disconnected from V_{DD}

Corollary: you can’t build positive logic, e.g., AND, with one CMOS gate

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>A·B</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

For CMOS gate:
- All inputs 0
  → nfets off, pfets on
  → output must be 1
- All inputs 1
  → nfets on, pfets off
  → output must be 0

Oops, output is also rising!

A=1, B rising...
CMOS Timing Specifications

Circuit:

Electrical model:

Waveforms:

time constant \( \tau = R_{PD} \cdot C_L \)

time constant \( \tau = R_{PU} \cdot C_L \)
Propagation delay ($t_{PD}$): An UPPER BOUND on the delay from valid inputs to valid outputs.

**GOAL:** minimize propagation delay!

**ISSUE:** keep capacitances low and transistors fast.
Contamination delay ($t_{CD}$): A LOWER BOUND on the delay from any invalid input to an invalid output

Do we really need $t_{CD}$?

Usually not... it’ll be important when we design circuits with registers (coming soon!)

If $t_{CD}$ is not specified, safe to assume it’s 0.
The Combinational Contract

\[ A \rightarrow B \]

\[
\begin{array}{c|c|c}
A & B & t_{PD} \\
0 & 1 & \text{propagation delay} \\
1 & 0 & \text{contamination delay}
\end{array}
\]

Notes:
1. *No Promises* during \( \gg \gg \gg \gg \)
2. Default (conservative) spec: \( t_{CD} = 0 \)
Acyclic Combinational Circuits

If NAND gates have a $t_{PD} = 4\text{ns}$ and $t_{CD} = 1\text{ns}$

$t_{CD}$ is the *minimum* cumulative contamination delay over all paths from inputs to outputs

$t_{PD}$ is the *maximum* cumulative propagation delay over all paths from inputs to outputs

$t_{PD} = \underline{12} \text{ns}$

$t_{CD} = \underline{2} \text{ns}$
One Last Timing Issue...

Recall the rules for combinational devices:

Output guaranteed to be valid when *all* inputs have been valid for at least $t_{PD}$, and, outputs may become invalid no earlier than $t_{CD}$ after an input changes!

Many gate implementations—e.g., CMOS—adhere to even tighter restrictions.
**What Happens In This Case?**

**CMOS NOR:**

- **Input A=1** is sufficient to determine the output.

**LENIENT Combinational Device:**

Output guaranteed to be valid when any combination of inputs sufficient to determine the output value has been valid for at least $t_{PD}$. Tolerates transitions -- and invalid levels -- on irrelevant inputs!

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<table>
<thead>
<tr>
<th>NOR:</th>
<th>A</th>
<th>B</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 1</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 0</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 1</td>
<td>0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Lenient NOR:</th>
<th>A</th>
<th>B</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 1</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>X 1</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 X</td>
<td>0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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Input A=1 is sufficient to determine the output.
Summary

• CMOS
  • MOSFETs behave as voltage-controlled switches
  • Only use NFETs in pulldowns, PFETs in pullups
  • Series/parallel pullup and pulldown switch circuits are complementary
  • CMOS gates are naturally inverting (rising input transition can only cause falling output transition, and vice versa).
  • “Perfect” VTC (high gain, $V_{OH} = V_{DD}$, $V_{OL} = GND$) means large noise margins and no static power dissipation.

• Timing specs
  • $t_{PD}$: upper bound on time from valid inputs to valid outputs
  • $t_{CD}$: lower bound on time from invalid inputs to invalid outputs
  • If not specified, assume $t_{CD} = 0$
  • Lenient gates: output unaffected by some input transitions

• Next time: Logic simplification, other canonical forms