Problem 1. Warmup (5 points)

(A) (2 points) Can the value of the sum 0xB3 + 0x47 be represented using an 8-bit 2’s complement representation? If so, what is the sum in hex? If not, write NO.

Hex representation of sum, or NO: 0xFA

Can the value of the sum 0xB3 + 0xB1 be represented using an 8-bit 2’s complement representation? If so, what is the sum in hex? If not, write NO.

0xB3 + 0xB1 = 0x164 which is too large for 8 bits

Hex representation of sum, or NO: 0x NO

(B) (1 point) You are given an unknown 5-bit binary number. You are then told that the first and last bits are the same. How much information have you been given?

Bits of information (number or formula): \(\log_2(32/16) = 1\)

(C) (2 points) What is the Hamming distance between the encodings for A and B? Using an encoding scheme with this Hamming distance, how many bits of error can be detected? How many bits of error can be corrected?

A: 010010
B: 110101

Hamming distance: 4

Number of error bits that can be detected: 3

Number of error bits that can be corrected: 1
Problem 2. Huffman Encoding (4 points)

For each of the probability distributions for symbols A-E, select the Huffman encoding tree or trees that could result from running Huffman’s algorithm on those probability distributions.

(A) \( p(A) = 0.3, \ p(B) = 0.3, \ p(C) = 0.2, \ p(D) = 0.1, \ p(E) = 0.1 \)

Huffman Tree(s) (1-3): 2

(B) \( p(A) = 0.6, \ p(B) = 0.1, \ p(C) = 0.1, \ p(D) = 0.1, \ p(E) = 0.1 \)

Huffman Tree(s) (1-3): 3

(C) \( p(A) = 0.5, \ p(B) = 0.15, \ p(C) = 0.15, \ p(D) = 0.1, \ p(E) = 0.1 \)

Huffman Tree(s) (1-3): 3

(D) \( p(A) = 0.5, \ p(B) = 0.2, \ p(C) = 0.15, \ p(D) = 0.05, \ p(E) = 0.1 \)

Huffman Tree(s) (1-3): 1
Problem 3. CMOS (6 points)

(A) (2 points) Given a function F defined by the truth table to the right, provide a minimal sum-of-products expression for F. Hint: Use a Karnaugh Map.

Minimal Sum-of-products Expression for F: \( \overline{A} + \overline{D} + \overline{B} \cdot \overline{C} \)

(B) (3 points) Which of the above CMOS pulldown circuits would implement F if the corresponding complementary pullup circuit was also provided? For each pulldown, select Yes if it is a valid pulldown for F, and No if it is not a valid pulldown for F.

| PD1 (Yes/No): | Yes | PD2 (Yes/No): | No | PD3 (Yes/No): | No | PD4 (Yes/No): | No | PD5 (Yes/No): | Yes |

(C) (1 point) Are all the implementations you selected for part (B) lenient?

A single CMOS gate is always lenient. All lenient (Yes/No): Yes
Problem 4. Static Discipline (7 points)

Ms. Anna Logge, founder at a local MIT start-up, has developed a device to be used as an inverter. Anna is considering the choice of parameters by which her logic family will represent logic values and needs your help.

The voltage transfer curve of a proposed inverter for a new logic family is shown to the right (spare copies of this diagram can be found below).

Several possible schemes for mapping logic values to voltages are being considered, as summarized in the incomplete table below. Recall that Noise Immunity (last row) is defined as the lesser of the two noise margins.

Complete the table by filling in missing entries. Choose each value you enter so as to maximize the noise margins of the corresponding scheme. If the numbers in a scheme can’t be completed such that the device functions as an inverter with positive noise margins, put an X in the entries for that column.

(complete table – 10 entries)

LNI’s Possible Logic Mappings:

<table>
<thead>
<tr>
<th></th>
<th>Scheme A</th>
<th>Scheme B</th>
<th>Scheme C</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OL} )</td>
<td>X</td>
<td>0.5</td>
<td>1</td>
</tr>
<tr>
<td>( V_{IL} )</td>
<td>2</td>
<td>1</td>
<td>0.5</td>
</tr>
<tr>
<td>( V_{IH} )</td>
<td>X</td>
<td>3</td>
<td>X</td>
</tr>
<tr>
<td>( V_{OH} )</td>
<td>X</td>
<td>5</td>
<td>X</td>
</tr>
<tr>
<td>Noise Immunity</td>
<td>X</td>
<td>0.5</td>
<td>X</td>
</tr>
</tbody>
</table>

\( V_{IL} = 2 \) leaves no possible choice for \( V_{OH} \)

\( V_{IL} < V_{OL} ! \)
Problem 5. Sequential Logic (8 points)

Consider the following sequential logic circuit. It consists of one input IN, a 2-bit register that stores the current state, and some combinational logic that determines the state (next value to load into the register) based on the current state and the input IN.

(A) (2 points) Using the timing specifications shown below for the XOR and DREG components, determine the shortest clock period, \( t_{CLK} \), that will allow the circuit to operate correctly or write NONE if no choice for \( t_{CLK} \) will allow the circuit to operate correctly and briefly explain why.

<table>
<thead>
<tr>
<th>Component</th>
<th>( t_{CD} ) (ns)</th>
<th>( t_{PD} ) (ns)</th>
<th>( t_{SETUP} )</th>
<th>( t_{HOLD} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>XOR2</td>
<td>0.15</td>
<td>2.1</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>DREG</td>
<td>0.1</td>
<td>1.6</td>
<td>0.4</td>
<td>0.2</td>
</tr>
</tbody>
</table>

Minimum value for \( t_{CLK} \) (ns): 6.2
or explain why none exists

\[ t_{CLK} \geq t_{PD,REG} + 2 \times t_{PD,XOR} + t_{SETUP,REG} = 1.6 + 2 \times 2.1 + 0.4 \]

(B) (4 points) Using the same timing specifications as in (A), determine the setup and hold times for IN with respect to the rising edge of CLK.

\[ 2 \times t_{PD,XOR} + t_{SETUP,REG} = 2 \times 2.1 + 0.4 \]
\[ t_{SETUP} \text{ for IN with respect to } \text{CLK}^\uparrow \text{ (ns)}: \ 4.6 \]

\[ t_{HOLD,REG} - t_{CD,XOR} + = 0.2 - 0.15 \]
\[ t_{HOLD} \text{ for IN with respect to } \text{CLK}^\uparrow \text{ (ns)}: \ 0.05 \]

(C) (2 points) One of the engineers on the team suggests using a new, faster XOR2 gate whose \( t_{CD} = 0.05 \text{ns} \) and \( t_{PD} = 0.7 \text{ns} \). Determine a new minimum value for \( t_{CLK} \) or write NONE and explain why no such value exists.

Minimum value for \( t_{CLK} \) (ns): none
or explain why none exists

Now \( t_{CD,REG} + t_{CD,XOR} \) is not greater than \( t_{HOLD,REG} \)

END OF QUIZ 1!