Please enter your name and Athena login name in the spaces above. Enter your answers in the spaces provided after each question. You can use the extra white space and the backs of the pages for scratch work. We can give partial credit only if your work is shown on the exam.

Problem 1. Virtual Memory (10 points)

Consider a Beta processor that includes a 32-bit virtual address, an MMU that supports 4096 \(2^{12}\) bytes per page, \(2^{24}\) bytes of physical memory, and a large Flash memory that serves as a disk. The MMU and the page fault handler implement an LRU replacement strategy.

(A) (2 Points) The designers are thinking about implementing the page map using a separate SRAM memory with \(L\) entries, where each entry has \(B\) bits. If the page map includes the standard dirty and resident bits, what are the appropriate values for the parameters \(L\) and \(B\)?

- Appropriate value for the parameter \(L\): _________
- Appropriate value for the parameter \(B\): _________

(B) (3 Points) If the designers decide to decrease the page size to 2048 \(2^{11}\) bytes but keep the same size virtual and physical addresses, what affect will the change have on the following architectural parameters? Use a letter “a” through “e” to indicate how the new value of the parameter compares to the old value of the parameter:

- (a) doubled
- (b) increased by 1
- (c) stays the same
- (d) decreased by 1
- (e) halved

- Size of page map entry in bits: _____
- Number of entries in the page map: _____
- Maximum percentage of virtual memory that can be resident at any given time: _____
(D) (4 points) A test program has been running on the Beta with a page size of $2^{12}$ bytes and has been halted just before execution of the following instruction at location 0x1234:

$$\text{ST(R1,0x34C8,R31) | PC = 0x1234}$$

The first 8 locations of the page table at the time execution was halted are shown below; the least-recently-used page (“LRU”) and next least-recently-used page (“next LRU”) are as indicated. Assume that all the pages in physical memory are in use. Execution resumes and the ST instruction is executed.

Please show the contents of the page table after the ST instruction has completed execution by crossing out any values that changed and writing in their new values. Note that the D and PPN fields for a non-resident page do not need to be specified.

(E) (1 point) Which physical pages, if any, need to be written to disk during the execution of the ST instruction in part (D)?

Physical page numbers written to disk or NONE: __________

Problem 2. Operating Systems (4 points)

Please implement the SNOOZE supervisor call handler for the Lab 7 operating system. To use SNOOZE, the user program first puts an integer time-of-day into R0, then executes the SNOOZE() SVC. The next instruction in the user program should be executed only when the time-of-day has reached (or passed) the time indicated in R0. When the user program resumes, the value in R0 should be 0. In the operating system, the time-of-day is maintained by an interrupt handler invoked by an IRQ signal asserted once per second. Your code should allow good CPU utilization by other running programs. Note that the user’s register “j” can be accessed at User.Regs[j]. Please add the appropriate lines of code to the SNOOZE handler below:

```c
SNOOZE_h() {
    if (GetTimeOfDay() >= User.Regs[0]) {
        
    } else {
        
    }
}
```
Problem 3. Interrupts and Real-time (7 points)

A particular real-time system has three interrupt handlers. The following table shows the maximum rate at which each interrupt occurs (rate), the time taken to execute each handler (service time), and the maximum allowable interval between the interrupt and completion of the handler (deadline). In your analysis, assume that A, B, and C interrupts can arrive at any time.

<table>
<thead>
<tr>
<th>Task</th>
<th>Rate</th>
<th>Service time</th>
<th>Deadline</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1/40ms</td>
<td>5ms</td>
<td>30ms</td>
</tr>
<tr>
<td>B</td>
<td>1/100ms</td>
<td>?ms</td>
<td>100ms</td>
</tr>
<tr>
<td>C</td>
<td>1/50ms</td>
<td>10ms</td>
<td>25ms</td>
</tr>
</tbody>
</table>

Please answer the following two questions assuming the system has a weak priority system.

(A) (1 point) What is the maximum service time for task B that still allows all constraints to be met?

Maximum service time for task B (ms): __________

(B) (1 point) Assuming a suitable service time for B, give a weak priority order for the tasks that meets the constraints. List the task with the highest priority first, the task with the lowest priority last.

Weak priority order for the tasks: _______________

Please answer the following two questions assuming the system has a strong priority system where task C has the highest priority and task B has the lowest priority.

(C) (2 points) What is the maximum service time for task B that still allows all constraints to be met?

Maximum service time for task B (ms): __________

(D) (3 points) Assume B’s service time is 10ms. For each task, what is the worst-case delay between the task’s interrupt and completion of the task’s interrupt handler?

Worst-case delay for task A (ms): __________

Worst-case delay for task B (ms): __________

Worst-case delay for task C (ms): __________
Problem 4. Semaphores (9 points)

The following pair of processes share the variable counter, which has been given an initial value of 10 before execution of either process begins:

```
Process A                                 Process B
...                                    ...
A1: LD(counter,R0)             B1: LD(counter,R0)
    ADDC(R0,1,R0)             ADDC(R0,2,R0)
A2: ST(R0,counter)                      B2: ST(R0,counter)
...                                    ...
```

(A) (3 points) If Processes A and B are run on a timesharing system, there are six possible orders in which the LD and ST instructions might be executed. For each of the orderings, please give the final value of the counter variable.

A1 A2 B1 B2: counter = __________  B1 A1 B2 A2: counter = __________
A1 B1 A2 B2: counter = __________  B1 A1 A2 B2: counter = __________
A1 B1 B2 A2: counter = __________  B1 B2 A1 A2: counter = __________

In the following two questions you are asked to modify the original programs for processes A and B by adding the minimum number of semaphores and signal and wait operations to guarantee that the final result of executing the two processes will be a specific value for counter. Give the initial values for every semaphore you introduce. For full credit, your solution should allow all execution orders that result in the required value.

(B) (3 points) Add semaphores (with initial values) so that the final value of counter is 12.

Semaphores: ____________________________

```
Process A                                 Process B
...                                    ...
A1: LD(counter,R0)             B1: LD(counter,R0)
    ADDC(R0,1,R0)             ADDC(R0,2,R0)
A2: ST(R0,counter)                      B2: ST(R0,counter)
...                                    ...
```

(C) (3 points) Add semaphores (with initial values), so that the final value of counter is not 13.

Semaphores: ____________________________

```
Process A                                 Process B
...                                    ...
A1: LD(counter,R0)             B1: LD(counter,R0)
    ADDC(R0,1,R0)             ADDC(R0,2,R0)
A2: ST(R0,counter)                      B2: ST(R0,counter)
...                                    ...
```

END OF QUIZ 4! Have a good summer...